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Design of Low Power Efficient Full Adder Using Six Transistor X-OR and Mux Circuit

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ABSTRACT

Full adders are the essential building square of ALU. ALU is a key unit of the chip and DSP. In the realm of innovation it has gotten to be important to develop new techniques to reduce the area and power consumption. This paper consists of a conventional CMOS full adder design and a proposed full adder design. The conventional CMOS makes use of 28 transistors which consumes lot of power and area as the transistor count is high. In order to reduce the transistor count, the proposed full adder is designed using transmission gate and complementary pass transistor logic technique. This circuit is implemented using six transistor XOR gates and the carry logic of the circuit is implemented using 2:1Mux. Optimized design of these logic gates increases the performance of VLSI systems as these gates are utilized as sub blocks in larger circuits. Three other low power adder circuits have been designed for better understanding and finally the resultant power and area efficiency are compared for all the adder circuits.

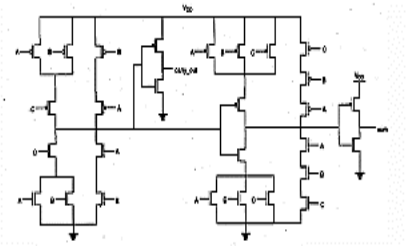
KEYWORDS: Transmission Gates (TG), MUX, Transistor count, XOR gates.

1. INTRODUCTION

In VLSI arrangement approaches power decrease is one of the crucial perspectives in light of the fact that a long battery life is required for cell phones and helpful contraptions, Power spread is growing as number of transistors additions on a lone chip. The equipment business has finished a remarkable improvement over the span of the last couple of decades, in a general sense in light of the quick advances in blend developments (IC) and immeasurable scale structures arrangement. Snake is a champion amongst the most fundamental parts of a processor, as it is used as a part of the quantity of juggling justification unit (ALU), in the coasting point unit, and for area period if there ought to emerge an event of store or memory access. In any CMOS VLSI circuit plots dynamic technique is the most basic part. . Move from either low to high („0" to „1") or on the other hand from high to low („1"to „0") both PMOS and NMOS transistors are ON for a constrained capacity to centre time. This results in short current heartbeat from VDD to GND. Current is in like manner required in charging and discharging the yield capacitive burden. The change from VDD to GND results in a "short out" spread that is liable to the information either rise time then again fall time and furthermore of burden capacitance and door design. Condition having no heap capacitance, the "short out" current is detectable. As the capacitive weight is extended, the charging or discharging current starts to lead the current drawn from the force supplies.

Conventional and proposed Designs of full Adder: 28 transistor ordinary CMOS outline was proposed utilizing transmission doors. In the wake of reenacting CMOS and pass transistors based full snake, looked at the normal force utilization. 6T based Full snake expended 98% less power contrasted with 28T ordinary CMOS full adder (Dhyanendra Singh Chandel, 2015). The proposed outline utilizes corresponding pass transistor logic strategy bringing about decrease of transistor number contrasted with the traditional CMOS plan. The two regularly utilized logic styles as a part of outlining full adders for CMOS that is the pass transistor logic procedure and the reciprocal pass transistor logic strategy were discussed. In pass transistor logic strategy, the essential inputs are utilized to drive the entryways of transistors and additionally source channel terminals of the MOSFET. The utilization of lessened number of the transistors gives lower capacitance. However there is an issue of limit voltage drop through NMOS transistor Logic which requires the utilization of swing rebuilding logic at the entryway yield. So we lean toward correlative pass transistor logic strategy. Integral CMOS logic style is a blend of two systems; the Pull up Network (PUN) and the Pull down Network (PDN). The Pull up Network comprises of PMOS transistors and Pull down Network comprises of NMOS devices. The capacity of Pull up Network is to give association between door yield and Vdd, at whatever time the yield of the entryway is intended to be high. Likewise, capacity of Pull down Network is to give association between entryway yield and GND at whatever time the yield of the door is intended to be low. The Pull up Network and Pull down Network are totally unrelated to each other. The clamor edge and engendering delay relies on upon the info designs. A full snake assumes an imperative part in numerous number-crunching units, for example, the viper, the multipliers, and the dividers. There have been numerous CMOS usage for the full adders. The Dual Domino logic full snake utilizes two sub circuits one for SUM and the other for CARRY (Goel, 2014). The Static vitality recuperation full viper utilizes multi limit system and the paired accuracy tree full snake utilizes twofold tree logic. The paired exactness tree full snake makes utilization of lessening of states system. At last after the usage of the considerable number of adders, the force utilization and territory proficiency are thought about for the majority of the plans.

Conventional Design of CMOS full adder: This logic cell uses 28 transistor based on regular CMOS structure (pull-up and pull-down networks). Complementary transistor pairs make the circuit schematic straight forward. CCMOS generates carry through a static gate .The advantage of using CCMOS is that it has layout regularity, high noise margins and stability at low voltage due to complementary transistor pair and smaller number of interconnecting wires and disadvantage is that it uses Cout signal to generate sum which produces an unwanted additional delay. It has weak o/p driving capability due to series transistors in output stage and consumes more power and large silicon area.



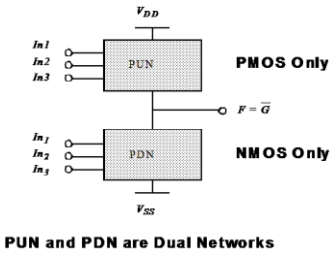


Figure.1.Conventional CMOS Design **Figure.2.Static CMOS**

Logic style of a circuit impacts its velocity, power dissemination, size and wiring many-sided quality. The circuit delay relies on the quantity of transistors in arrangement, transistor sizes and wiring capacitances. Strength regarding voltage and transistor scaling and in addition fluctuating procedure, working conditions and similarity with encompassing hardware are critical angles affected by actualized logic style. However, vast clock burdens and high flag move exercises because of pre-charging instruments result in unnecessary force dissemination. In this manner, As these pass transistor multiplexer structure require correlative control flags along these lines, double rail logic is utilized. Design of Pass transistor is not as straight-forward and productive as reciprocal CMOS, because of their unpredictable structure Cheng, 2013. It comprises of n-channel transistor and in addition p-channel transistor with partitioned entryway associations and regular source and deplete associations. The control sign is connected to door of n-channel transistor and its supplement is connected to the entryway of p-channel transistor. By consolidating the qualities of pchannel transistor and in addition n-channel transistor, it can pass logic "1" and logic "0" productively with no contortion. At each point in time (with the exception of amid the exchanging drifters) every door yield is associated with either VDD or VSS by means of a low unsettled Simulation of circuits might be required to guarantee sufficient execution. In this logic either nMOS or Pmos is adequate to perform logic operation, along these lines, number of transistors and i/p load diminishes furthermore the Vdd to gnd ways are wiped out .Static and element sorts of pass transistor logic exist, with contrasting properties concerning speed, power and low-voltage operation. Chiou-Kou Tung, 2013 Because reciprocal inputs are regularly required to control pass transistors, extra logic stages are required. Because of high number of transistors the transistor tally is high and the force utilization is more. along these lines, we incline toward proposed model which utilizes reciprocal pass transistor logic strategy and is more power and territory productive contrasted with the customary CMOS outline of full adder.

Proposed Design of Full Adder: The proposed full adder uses complementary pass transistor logic and transmission gate, Which follows the Boolean equation as shown below where X,Y,Z are the inputs ,SUM and CARRY are the outputs of full adder.

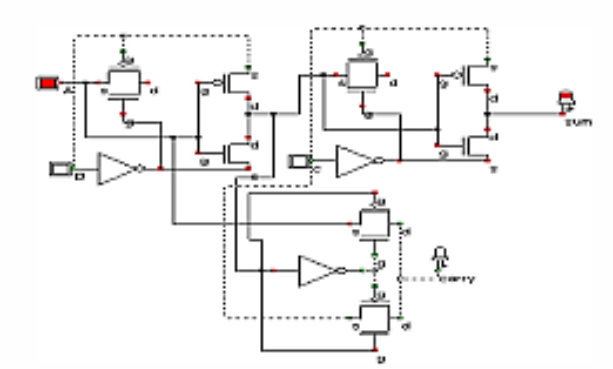


Figure.3. Proposed Full Adder

$$\mathrm{SUM} = \bar{X}\bar{Y}Z + \bar{X}Y\bar{Z} + X\bar{Y}\bar{Z} + XYZ$$
$$\mathrm{CARRY} = \bar{X}YZ + X\bar{Y}Z + XY\bar{Z} + XYZ$$

The exclusive–OR (XOR) and exclusive–NOR (XNOR) gates are the basic building blocks of a full adder circuit. The XOR/XNOR gates can be implemented using AND, OR, and NOT gates with high redundancy. In CPL, the given function is implemented by two pass transistor networks with one implementing the function f and the other implementing f'. CPL implements differential logic as every variable is represented in its true and complementary form Ahmed, 2012. The logic structure of CPL is shown-

CPL experienced issues of sign debasement when the sign is gone through a progression of transistor, its quality is corrupted by one Vt (limit voltage) Anjali Sharma, 2012. The issue of limit voltage drop can be killed by utilizing level rebuilding circuit that comprises of exceptional kind of inverters .with a specific end goal to drive different entryways of the same sort, it must create the yields likewise in genuine and supplement shapes. So every sign is conveyed by two wires. Henceforth CMOS yield inverters with pass transistor logic to give correlative inputs and yields. To create aggregate out and do flag are utilized as a part of this viper cell along these lines, it is not reasonable for low power applications. Point of preference of CPL is that it is speedier than CCMOS full snake. To decrease power utilization of CPL SR-CPL (swing restored CPL is utilized to overcome multi-edge voltage drop) and LCPL (single rail pass transistor logic) logics are utilized. A transmission door has three inputs called source, n-entryway and p-door. It additionally has one yield called drain (Chiou-Kou Tung, 2013). In the event that, then again, the control signal X is low, then both transistors will be off, and the way between the IN and OUT will be an open circuit. The primary point of preference of the CMOS transmission door contrasted with NMOS transmission entryway is to permit the information sign to be transmitted to the yield without lessening in the limit voltage. It gives full swing yield in this way, its utilization give better speed in CMOS circuit however there is no confinement amongst info and yield. In the Transmission Gate CMOS Full Adder, it utilizes 20 transistors. It has great deferral, power dissemination and PDP than CCMOS and CPL. It gives preferable rate over static CMOS, CPL and requires less number of transistors. It has high number of interior hubs which prompts an expansion in parasitic capacitance .In extensive number-crunching circuits it gives poor performance (Sathiyabama, 2012). Extra cushions are required at every yield because of their week driving capacity which expands power utilization and range. In the XOR and transmission door plan, the viper cell utilizes 18 transistors for snake operation. A XOR door and transmission entryways are utilized as a part of mix for its outline. It is otherwise called 18T adder. The half total is created by XOR entryway and transmission doors will produce the whole and convey yield. This viper cell possesses less region. It has low movement figure so expends less power. The convey logic is executed with 2:1 Mux. The operation of the multiplexer can be seen effortlessly, if the control info S is logic high, then the base TG will direct and the yield will be equivalent to the information (Sajid B, 2012). In the event that the control sign is low, the base TG will kill and the top TG will interface the info A to the yield hub.

Dual Threshold domino logic Full Adder: In this adder, the proposed full adder is divided into two Sub circuits. One is the circuit for SUM operation, and the other is the circuit for CARRYOUT operation. In this adder, not only the dynamic power consumptions but also the static power consumptions are considered. We apply the multi-threshold CMOS (MTCMOS) technology in this design to reduce the static power consumption. Besides, we combine the concept of domino logic and cross-coupled XOR in this design to achieve a high-speed full adder.

SUM circuit is composed of two XOR gates. The XOR gate is modified from the cross-coupled version by replacing the NMOS portion with a clock gated NMOS. In this circuit, the PMOS transistors receive the input signal A, B, and Cin. The operation of this circuit can be divided into two phases: the IDLE PHASE and the EVALUATING PHASE. In the IDLE PHASE, the clock signal CLK is 'logic 1', and the output signal SUM will be 'logic 0'. In the EVALUATING PHASE, the clock signal CLK is 'logic 0', and the corresponding output signal SUM will be evaluated according to the input signals A, B, and C. The core of this circuit is the domino logic that implements the function of CARRYOUT (Shiv Shankar Mishra, 2011). This circuit will stay in standby phase when the clock signal CLK is 'logic 1'. It will turn in the evaluating phase if the clock signal CLK is 'logic 0'.For the high-speed operation, the inverter I1 is designed in multi-threshold methodology where a low-Vt PMOS transistor is connected with a high-Vt NMOS transistor such that the 'logic 0' can pass the inverter at a higher speed.

Static Energy Recovery Full Adder (SERF): Aggregate is produced by two XNOR doors and Cout is created by two transistors multiplexer piece. The single piece full viper utilizing proposed XNOR entryways with eight transistors has been actualized and for multiplexer area run of the mill estimations of width (Wn and WP) 1.0μm and 2μm for NMOS and PMOS transistors have been brought with door length of 0.35μm.The cell utilizes just 10 transistors and it doesn't require rearranged inputs (Manoj Kumar, 2011). The charge put away at the heap capacitance is reapplied to the control gates. The blend of not having an immediate way to ground and the re-use of the heap charge to the control door makes the vitality recouping full snake a vitality effective outline. To the best of our insight this new outline has the most reduced transistor mean the complete acknowledgment of a full viper. The mix of low power and low transistor number makes the new SERF cell a suitable alternative for low power plan.

Binary Decision Tree Full Adder: Full Adder is a logic circuit that adds a pair of corresponding bits of two numbers expressed in binary form and also any carry from a previous stage producing a sum with a new carry. Hence, it is also called a three input adder. Mathematically,

$$Sum = x \oplus y \oplus z$$
$$Carry = xy + yz + zx$$

The full adder equations are used to design a binary decision tree. Each node in the tree can be replaced by a 2:1 Mux.

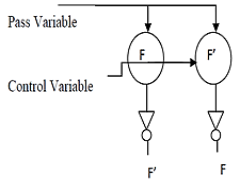


Figure.4.CPL logic Structure

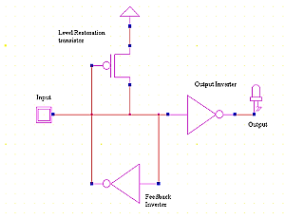


Figure.5.Cpl Restoring Logic

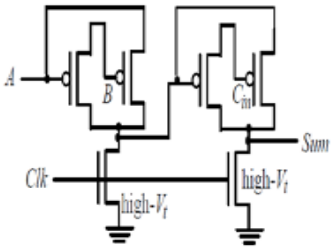


Figure.6.Circuit for sum

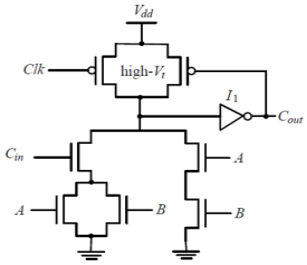


Figure.7.Circuit for carry

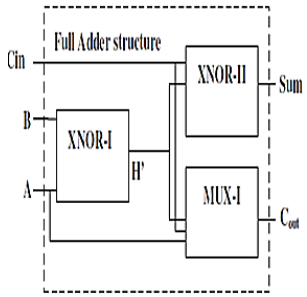


Figure.8.Block diagram for SERF

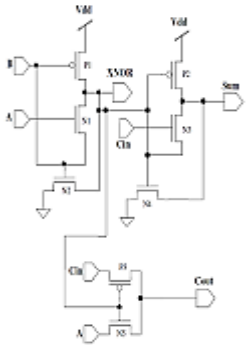


Figure.9.Full adder using two XNOR gates and multiplexer

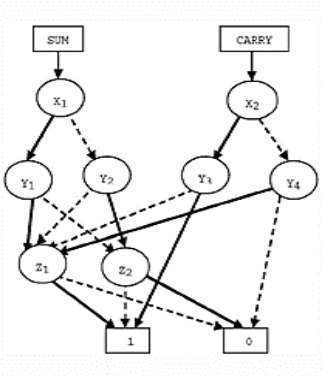


Figure.10.Binary decision tree for I bit adder

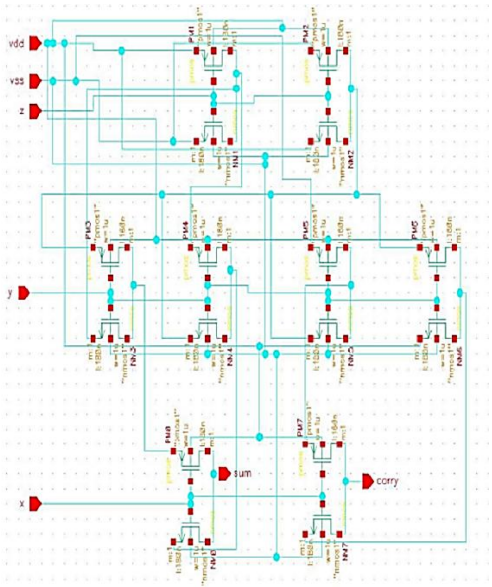


Figure.11.I bit full adder using 2T 2: I mux

Here X1 is used to represent SUM and Y1 and y2 is used for performing the two XOR functions in sumY3 and Y4 are used to implement the AND operation in the carry logic Z1 and Z2 perform the OR operation in the carry logic and the corresponding output for sum and carry is obtained .Thus using this methodology the number of internal transition states are reduced. Each node in the tree can be replaced by 2: 1 mux. So, firstly a two

transistor 2: 1 mux is designed. Using the 2: 1 mux each node in the binary tree is replaced by it. Using this 2: 1 mux the sum and carry of the 1 bit full adder is formed as shown in the figure above.

2. RESULTS AND DISCUSSION

All the full viper outlines can be effectively actualized in the Tanner EDA programming. They are executed utilizing Schematic Editor(S-EDIT), T-Spice and Waveform Editor (W-EDIT). Schematic manager is an effective configuration catch and examination bundle that can create net rundown straightforwardly usable in T-Spice recreations. T-Spice performs quick and precise reenactment of simple and blended simple/advanced circuits. The test system incorporates the most recent and best gadget models accessible, and also coupled line models and backing for client characterized gadget models through tables or C capacities. W-Edit shows T-Spice recreation yield waveforms as they are being created amid reproduction after reenactment the relating waveforms for all the snake outlines are acquired.

Table.1. Area and Power Comparisons for adder design

Type of Adder	Area	Power
Existing Model	28 Transistors	1.6302mw
Proposed Model	18 Transistors	1.07095mw
Dual Threshold Domino logic	15 Transistors	1.18928mw
Static Energy Recovery Full Adder	10 Transistors	1.11407mw

From the comparison table of all the Adder designs, we can conclude that the proposed full adder using 6 transistor XOR gates and one 2:1 mux consumes the least power and is considered to be the most efficient adder.

3. CONCLUSION

This paper presents various logic styles have been compared taking full adder as a reference circuit and power dissipation and delay as reference parameters and different methods of implementing full adder using different types of logic styles have been discussed ,their corresponding results have been summarized.. It presents an area and power efficient technique to design a full adder, using transmission gate and 2:1 mux in order to reduce transistor count. The power dissipation is least in the case of transmission gate transistor implementation of full adder due to reduced load capacitance. Most of the conventional CMOS adders have been designed using 28 transistors which are very high. As number of transistors increases results in high power consumption. To overcome this problem, the proposed full adder has been designed using less number of transistors (18 Transistors) to improve the power and area simultaneously. Finally the power consumption and area efficiency results for all the adders are compared for better understanding.

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